REMARKS

Claims 1-45 were presented for examination and were pending in this application. As listed above in the claims section, Applicant herein adds claims 46 and 47. Applicant now requests reconsideration and addresses Examiner's comments below.

In paragraph 2 of the Official Action, Examiner rejected claims 1 to 45 under 35 USC 103(a) as being unpatentable over Boggs (US 7,051,329) in view of Kalafatis (US 6,785,890). Applicants respectfully traverse the rejections. In summary, while the claims are directed to

Claim 1 is directed to a network processor. The network processor comprises:

> a fetch control unit, having an input coupled to receive an execution feedback signal with information related to a plurality of threads on a per thread basis, the fetch control unit generating an instruction fetch sequence based on the execution feedback signal; and
>
> an instruction cache, having an input coupled to an output of the fetch control unit, the instruction cache dispatching instruction data responsive to the instruction fetch sequence.

Thus, the fetch control unit generates an instruction fetch sequence based on information related to a plurality of threads within the execution feedback signal. Advantageously, the fetched instructions address needs of the actual executions of particular threads downstream.

Boggs discloses an apparatus for managing resources in a multithreaded processor. (Abstract). More particularly, Boggs discloses a trace delivery engine 230 that feeds back a stall signal to microinstruction translation engine 224. (See Figure 2). The stall signal causes the trace delivery engine 230 to stall until the stall conditions are cleared. (See 11:39-44). Meanwhile, Kalafatis discloses a system to perform threads switching responsive to a lack of instructions for a particular thread. (See Abstract). Similar to Boggs, Kalafatis discloses a trace feedback engine 60 and a microinstruction translation engine 54. (See Figure 2). The microinstruction translation engine 54 feeds back an instruction fetch request signal 50 to a

memory execution unit 42, and the micrinstruction translation engine 54 includes an instruction streaming manager 106 with two threads. (See Figure 3).

However, neither Boggs nor Kalafatis teaches or suggests the elements of the invention as recited in claim 1. Specifically, claim 1 recites a fetch control unit that generates an instruction fetch sequence based on information about a particular thread. Examiner acknowledges that Boggs fails to disclose an execution feedback signal with information related to a plurality of claims. (OA, para. 4). It follows that Boggs fails to disclose generating an instruction fetch sequence based on the execution feedback signal. While Examiner relies on Kalafatis for the general concept of thread switching information, Kalafatis fails to cure the deficiencies of Boggs. In Kalfatis, the thread switching signal and subsequent thread switch is responsive to a lack of instructions for a particular thread. (See 9:45-52). Claim 1 and Kalafatis are directed towards different parts of the processing pipeline (i.e., claim 1 is directed towards instruction fetching and Kalafatis is directed towards instruction decoding for execution). In other words, claim 1 generates an instruction fetch sequence to proactively retrieve instructions based on a thread's condition, whereas Kalafatis reactively issues an instruction based on thread stalls. Thus, neither Boggs nor Kalafatis discloses a fetch control unit that generates an instruction fetch sequence based on an execution feedback signal.

Becauase neither Boggs nor Kalafatis disclose generating an instruction fetch sequence as recited, neither reference can disclose an instruction cache that dispatches instructions responsive to the instruction fetch sequence.

Applicants submit that claim 1 is patentable over Boggs and Kalafatis either alone or in combination for at least the above reasons. Furthermore, claims 2 to 45 and new claims 46 and 47, to the extent that they include similar limitations, are patentable for at least the same reasons.

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CONCLUSION

In sum, Applicant respectfully submits that the claims as presented herein, are patentably distinguishable over the cited reference (including references cited, but not applied). Therefore, Applicant requests reconsideration and allowance of these claims.

In addition, Applicant respectfully invites Examiner to contact Applicant's representative at the number provided below if Examiner believes it will help expedite furtherance of this application.

RESPECTFULLY SUBMITTED,
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